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Claims

I Claim:

5 1. A method for forming a low capacitance isolation
tub comprising the steps of:

 providing a region of semiconductor material;

 forming a plurality of shapes in the region of
semiconductor material, wherein the shapes are free
10 standing, and wherein adjacent rows of shapes are offset
from each other; and

 exposing the plurality of shapes to an ambient that
includes a chemical species that reacts with the plurality
shapes to form the low capacitance isolation tub.

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 2. The method of claim 1 wherein the step of exposing
includes thermally oxidizing the plurality of shapes to form
a silicon oxide isolation tub.

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 3. The method of claim 1 further comprising the step
of forming a boundary around the plurality of shapes,
wherein the boundary includes a recessed portion.

 4. The method of claim 1 wherein the step of exposing
25 includes consuming substantially all of the plurality of
shapes.

 5. The method of claim 1 further comprising the step
of forming a passive device over the low capacitance
30 isolation tub.

 6. The method of claim 1 wherein the step of forming
the plurality of shapes includes etching exposed portions of
the region of semiconductor material.

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7. The method of claim 6 wherein the step of etching includes etching to a depth from about 6 microns to about 10 microns.

5 8. The method of claim 6 wherein the step of etching includes reactive ion etching.

9. The method of claim 1 wherein the step of providing the region of semiconductor material includes
10 providing a region comprising silicon.

10. A process for forming an integrated circuit device including the steps of:

forming a matrix of shapes within a semiconductor
15 layer, wherein the matrix of shapes comprises offset rows;
and

forming a dielectric region within the matrix of shapes.

20 11. The process of claim 10 wherein the step of forming the matrix of shapes includes forming a matrix of squares.

12. The process of claim 10 wherein the step of
25 forming the dielectric region includes oxidizing the matrix of shapes.

13. The process of claim 12 wherein the step of oxidizing forms a nearly continuous silicon oxide tub.

30 14. The process of claim 10 further comprising the step of forming a passive component over the dielectric region.

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15. The process of claim 10 further comprising the step of forming an isolation trench in the region of semiconductor material.

5 16. The process of claim 10 further comprising the steps of:

forming a dielectric layer on sidewalls of the matrix of shapes; and

10 forming a polycrystalline semiconductor layer over the dielectric layer.

17. The process of claim 10 wherein the step of forming the matrix of shapes includes forming a matrix of shapes wherein shapes in a first row have a first spacing, and wherein the shapes in the first row have a second spacing from shapes in a second row, and wherein the second spacing is less than the first spacing.

18. A semiconductor device comprising:
20 a region of semiconductor material; and
a dielectric tub comprising a matrix of shapes, wherein adjacent rows of shapes are offset.

19. The device of claim 18 wherein the dielectric tub
25 comprises oxidized silicon shapes.

20. The device of claim 18 wherein the dielectric tub includes a boundary having a recessed portion.